CEITEC – Central European Institute of Technology, Brno University of Technology would like to inform you about the on-coming lecture:

Ing. Pavel Neužil, Dr., DSc. (CEITEC BUT)

A new way to create IC/MEMS layout

18/1/2017

**Meeting Room S2.02
CEITEC BUT, Building "S"
Brno, Purkyňova 123**

Wednesday, 13:00

Conventional way to design IC, MEMS of microfluidic chips using full custom design is based on dedicated software such as Virtuoso from CADENCE, L-Edit by Tanner Research, K-Layout and others. Regardless of the software, researchers are drawing structures and then they convert the layout into gds format and send it to mask making tools such as Heidelberg DWL or e-beam writer. The problem starts once the layout has to be modified and one at that moment one can distinguish between good and bad layout.

I would like to give a short introduction into a modern way of GENERATING layout. It is based on a Java script parameterized structures. What one has to do to create a layout is to write a simple text file and in a few clicks at a PC to generated the layout. Each structure (cell) is represented by a single line of a text with parameters. The text file containing entire design can be hierarchical as any design in all professional layout editors making the total file short and easily editable.

So the way making design is following: first one has to choose structures from a file, ^C ^V them into text editor, replaced parameter names with actual values, create instances the same way, add labels, click "generate gds" and check the output layout. If there is a problem, go into the text file, modify parameters and generate new gds.

I personally know how to use Virtuoso from Cadence and since I have this tool I have not touch the Cadence and I have no intention of using Cadence in future.